APPLICATION NOTE

AN717

Functional enhancements from P51XA-G3 to PXA-G3 16-bit microcontrollers

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BACKGROUND

Philips Semiconductors manufactured P51XA-G37 devices, through 1998. Since then the P51XA-G37 devices have been replaced by PXA-G37 devices utilizing a different process technology. At that time, functional changes were implemented to improve the performance. **These changes in the PXA–G37 are in the area of timers and UART buffering. In some applications utilizing P51XA UARTs, the UART functional enhancements may require minor software changes.**

FUNCTIONAL IMPROVEMENTS

Timer Mode 3

The P51XA implementation of the Timer 0 used the upper half of Timer 0 to provide the baud rate when Timer 0 is in mode 3.

- The PXA implementation changed this to allow the baud rate to come from Timer 1. Timer 0 in mode 3 functions as two separate 8–bit timers, the second of which takes over register bits and the interrupt flag from Timer 1. Timer 1 continues to be usable as a baud rate generator. This allows the XA–G3 to provide 4 “functional” timers in applications where this feature is required.

Static Operation

- P51XA implementation of the XA–G3 required the external clock input to be stopped in a specific state in order for operation to be resumed correctly.
- PXA implementation allows an external clock to be stopped in any state with the ability to resume operation by restarting the clock.

ESWEN Bit

The XA architecture incorporates support for multi–tasking through two modes – namely the System/Supervisor and the User/Application modes. Applications that intend to restrict a User mode “Write through ES” can do so by re–setting the ESWEN bit to a 0.

- P51XA devices could potentially block some writes into the register file only when all the following conditions were met:
  a. Not in Page Zero Mode
  b. User mode active
  c. ESWEN set to a “0”
- PXA devices do not display this behavior.

Enhancements

- The P51XA UARTs transmitter is not double buffered.
- The PXA UART transmitter AND receiver are double buffered. Allowing fast data transmission with no gaps between bytes and with less critical timing of the interrupt service routine.

DIFFERENCES IN THE INTERRUPT TIMING BETWEEN THE TWO IMPLEMENTATIONS

- For the PXA UART implementation, when multiple bytes are being transmitted, the timing of interrupts is now different than on the P51XA. If the PXA double buffering is being used, this occurs at the beginning of the message.
- An “extra” interrupt occurs at the beginning of message transmission (immediately when SBUF is loaded) if the transmit shift register is not currently shifting out another character.
- This “extra” interrupt signals the user that the double buffered UART can now be loaded with an additional character.
- This “extra” interrupt (compared with the P51XA’s UART) should be discarded when using the UART in a manner which duplicates the P51XA single buffered UART transmission.

HOW TO CONVERT THE PXA–G3 UART TO A SINGLE BUFFERED TRANSMITTER

To convert P51XA–G3 software into PXA–G3 single buffered operation, the interrupt service routine must be changed slightly. The Interrupt service routine requires changes where the Transmitter interrupt flag: (TI_0 or TI_1) is cleared.

To force single buffered operation, an instruction that clears the TI flag is added at a location following when data is written to SBUF. This should be immediately after the write to SBUF. If system interrupts are enabled, it will be necessary to disable maskable interrupts so that a higher priority interrupt cannot occur between the write to SBUF and the clearing of the TI flag.

This can be done by clearing the EA bit before writing SBUF and setting EA back to “1” after the TI flag is cleared. Care must be taken that the TI interrupt flag is always cleared prior to exiting the interrupt service routine, whether or not additional data is transmitted.

If the UART is operated in either of the 9–bit modes (Mode 2 or Mode 3) the user should force the UART to revert to single buffered operation. This is necessary since the actual UART (SBUF) is double buffered but the 9 th bit, TB8 (contained in SCON), is not double buffered.

USING THE PXA–G3’S UART AS A DOUBLE BUFFERED TRANSMITTER

If double buffering is desired, the clearing of the TI flag must be done prior to writing additional data to SBUF. If the UART shift register is idle, a transmit interrupt will occur immediately and a second byte may be written to the UART while the first one is being transmitted.

Additional interrupts will occur as bytes complete transmission and the second UART buffer becomes available. As previously mentioned, this is needed when single buffered operation is forced, but it also allows tracking the completion of a message transmission if desired. Care must be taken in the interrupt service routine to insure that the exact number of interrupts does not cause erroneous operation, since this can vary depending on how “tightly” the characters are spaced when transmitted. For example, with the single buffered UART, 4 characters will always generate 4 transmit interrupts.

With the double buffered UART, 4 characters can generate 5, 6, 7, or 8 transmit interrupts depending on whether they are transmitted in a tight sequence or not.

The rule for the double buffered UART is that an interrupt is generated whenever SBUF is written to while the UART transmitter is idle (to allow the second buffer to be written), and when a

character completes transmission. When the UART is not allowed to become idle between characters, there is one extra interrupt when the first character of a stream is written. If the transmitter becomes idle between every character, then there are two interrupts generated for every character.

For the PXA UART If the UART shift register is idle when SBUF is loaded with the character, an “additional” transmit interrupt will occur immediately. Otherwise, every character will generate a “standard” transmit interrupt when it’s finished shifting out of the UART.

PRODUCT SUPPORT

Please direct questions regarding the P51 and PXA differences to the Microcontroller Applications Group via either the XA Help Line at **(408) 991–6000** or via by sending mail to **xa_help.svl@philips.com.**

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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